PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)
Makoto Yamamoto et al.	)
	) **Art Unit: 2815**
Serial No. **10/805,822**	)
(Divisional of 10/014,949 filed October 26, 2001)	)
Filed: **March 22, 2004**	) **Examiner: Wojciechowicz, Edward Joseph**
For: **Method of Fabricating Semiconductor Integrated Circuit**	) Attorney Docket No.: 44471/298721

I hereby certify that this correspondence is being deposited with the United States Postal Service as certified first class mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

05/24/2005

Janie Wilkins

Janie Wilkins

AMENDMENT AFTER ALLOWANCE UNDER 37 CFR 1.312

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Subject to the approval of the Examiner, please enter the following amendments.

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.